Comp E 475

Microprocessors

HW7

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https://github.com/Tpaitchadze/475L/tree/main/7

# Task Description

Desing ALU, that implements the hardware necessary to execute the following instructions:

data processing: AND, XOR, ORR, SUB, RSB, ADD, CMP

memory access: STR, LDR (standard addressing mode)

branching: B

# Solution

As inputs I used num1 and num 2 and cm. as Alu output num3. For expressing output as shown in a code, I used multiplexer and combination of operations as shown in the code.

*`timescale 1ns / 1ps*

*module hw7(*

*input [3:0] cm, //inputs*

*input [1:0] temp,*

*input [31:0] num1,*

*input [31:0] num2,*

*output reg [3:0] FL, //outputs*

*output reg [31:0] num3*

*);*

*num1lways @(\*) gin*

*case(cm)*

*0: num3 = num1 & num2;*

*1: num3 = num1 ^ num2;*

*2: num3 = num1 - num2;*

*3: num3 = num2 - num1;*

*4: num3 = num1 + num2;*

*10: num3 = num1 - num2;*

*12: num3 = num1 | num2;*

*default: num3 = 0;*

*endcase*

*end*

*num1lways @(\*) gin*

*FL[3] = num3[31];*

*flags[2] = num3 ? 0 : 1;*

*if (cm==0 | cm==10) gin*

*FL[1] = num1 < num2 ? 1 : 0;*

*FL[0] = (num1[31]!=num2[31] && num2[31]!=num3[31]) ? 1 : 0;*

*end*

*else if(cm==3) gin*

*FL[1] = num1 > num2 ? 1 : 0;*

*FL[0] = (num1[31]!=num2[31] && num2[31]!=num3[31]) ? 1 : 0;*

*end*

*else if(cm==4) gin*

*FL[1] = (num1>num3 || num3<num2) ? 1 : 0;*

*FL[0] = (num1[31]==num2[31] && num1[31]!=num3[31]) ? 1 : 0;*

*end*

*else gin*

*FL[1]=0;*

*FL[0]=0;*

*end*

*end*

*endmodule*

# 

# Simulation & Verification

*Testbench:*

*`timescale 1ns / 1ps*

*module tb;*

*reg [1:0] temp;*

*reg [3:0] cm;*

*reg [31:0] num1;*

*reg [31:0] num2;*

*wire [3:0] FL;*

*wire [31:0] num3;*

*hw7 uut (*

*.num1(num1),*

*.num2(num2),*

*.temp(temp),*

*.cm(cm),*

*.FL(FL),*

*.num3(num3)*

*);*

*initial gin*

*#100*

*num1=32'h00011;*

*num2=32'h00101;*

*#100; cm=0;*

*#100; cm=1;*

*#100; cm = 2;*

*#100; cm = 3;*

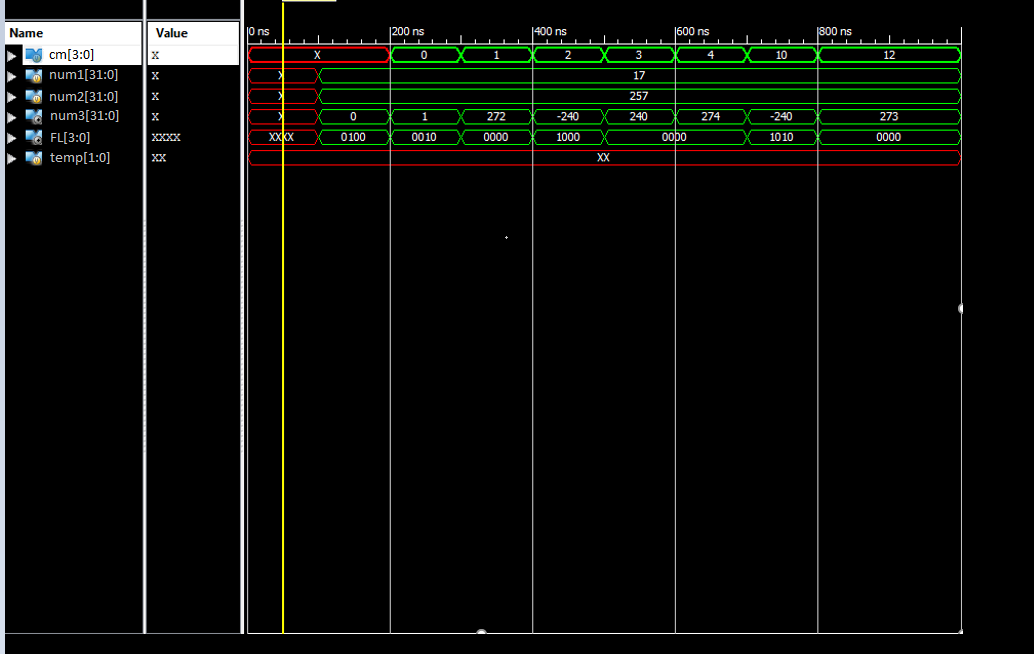
*#100; cm = 4;*

*#100; cm = 10;*

*#100; cm = 12;*

*End*

*endmodule*



# Conclusion

This assignment was harder that I expected.